REMARKS

Attached hereto is a marked-up version of the changes made by the current amendment with the title page captioned **"Version with markings to show changes made."**

Claims 1,2, 8-10, 16, 17 have been amended and new claims 18-22 have been added. No new matter has been added.

Claims 1 and 16 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Middelhoek et al in view of Yoshimi. Middelhoek et al disclose a memory cell for an electrically programmable semiconductor memory having a channel region disposed between source and drain regions, with a floating gate 11 disposed above a portion of the channel region. In addition, a control gate 12 is disposed above the floating gate, and an erase gate 14 has a portion overlying the channel region as well as a part of the floating gate. As pointed out by the Examiner, Middelhoek et al inter alia

> "...do not teach the limitation of providing a controlled gate having a first portion disposed over a portion of the substrate and being separated by said second insulating layer, a second portion formed over a first one of said side walls of said floating gate and a third portion formed over at least a portion of said top surface of said floating gate, said second portion having a surface substantially parallel to and opposing said first sidewalls."

Yoshimi discloses an electrically erasable non-volatile semiconductor memory device, which is provided with a floating gate FG, a control gate CG, and an erase gate 15. It is of interest to note that the floating gate spans completely across the channel region separating the drain 9 from the source 8, and that the control gate CG resides entirely over the source/drain region 8 and the top of the floating gate FG. Accordingly, although Yoshimi discloses a control gate structure that on first impression appears similar to Applicants' control gate, the disclosed device clearly does not meet Applicants' recited limitation

"a control gate having a first portion disposed over a portion of said channel region".

Applicants therefore respectfully traverse the rejection.

As is clearly evidenced in Fig. 10 of Middelhoek et al, the control gate 12 does not in part overlie the channel region of the device and instead lies directly over the floating gate 11.

The fact that the Middelhoek et al erase gate 14 depicted in Fig. 10 bears some physical resemblance to Applicants' control gate does not suggest the benefits disclosed by Applicants in providing a control gate having a portion which over lies the channel region, a portion which faces a side wall of the floating gate, and a portion which overlies the floating gave. Furthermore, the showing by Yoshimi likewise does not disclose Applicant's form of control gate since Yoshimi's control gates CG do not have any portion thereof lying directly over a channel region. In fact, the only portion of Yoshimi's control gate CG not lying directly over the floating gate FD is positioned directly over the source/drain region 8. There is thus no teaching in either reference that would lead one skilled in the art to modify the device of Middelhoek et al to include the particular control gate structure recited by Applicants in claims 1 and 16. Moreover, there is no teaching in either reference that would lead one to modify the invention of Yoshimi to provide a result that would meet the recitations of Applicants' claims 1 and 16. Applicants therefore request reconsideration of the rejection.

Claims 2, 8-10 and 17 were rejected under 35 U.S.C. 103 (a) as being unpatentable over Middelhoek et al in view of Yoshimi, and further in view of Chang. Chang discloses a flash EEPROM cell employing a sidewall polysilicon spacer as an erase gate. The Chang structure, to the extent that it is relevant, is almost identical to the Middelhoek et al structure in that it discloses a floating gate 103 with an overlying control gate 101, and has an erase gate 122 disposed to the side of the floating gate and control gate. It is of interest to note that, for example, Chang's Fig. 1f is substantially identical to the Middelhoek et al figure 10. Accordingly, Applicants repeat the above arguments and submit that there is no combination of Chang, Yoshimi and Middelhoek et al that is capable of meeting the above mentioned recitations of Applicants' claims . Reconsideration of the rejection is respectfully solicited .

Claims 1 and 16 have been rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35U.S.C. 103(a) as obvious over Van Houdt et al. Van Houdt et al disclose a High Injection MOS (HIMOS) flash EEPROM cell consisting in a split-gate structure and a coupling capacitor between the floating gate and an additional program gate in order to provide an enhanced injection efficiency. The electron injection is controlled by a control gate CG at the source side and the corresponding channel acts simultaneously as a select device in order to

prevent over erasure. The Examiner treats the program gate PG in Van Houdt et al as the erase gate. But column 9, line 20, it is stated that

> "Since the coupling factor between the program gate and the floating gate is in the order of 50% or more, the coupling factor between the control gate and the floating gate is automatically minimized in a proper design. This means that a high control-gate voltage will create a high electric field in the polyoxide layer between the control gate and the floating gate. Because of the well-known field enhancement effect at the upper floating gate surface, this field becomes large enough to enable the electrons, stored on the floating gate, to tunnel through the polyoxide layer towards the control gate."

This means that large voltage drop can not be developed between the program gate (PG) and the floating gate (FG). Therefore, tunneling erase between the PG and FG is unlikely. Accordingly, the PG does not function as the erase gate in the same sense as Applicants' invention in which the tunneling erase takes place between the erase gate and the floating gate. More specifically, the Van Houdt et al disclosure neither anticipates nor renders obvious Applicants invention as recited in claims 1 and 16 because, inter alia, it does not meet the recited limitation

> "whereby during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process".

Applicants therefore respectfully request reconsideration of the rejection.

New claims 18-22 describe Applicants' invention in terms of a semiconductor memory cell and contain descriptive language similar to that used in the existing claims. Applicants assert that these claims are allowable for the same reasons set forth above with respect to claims 1,2, 8-10, 16, 17, and entry thereof is respectfully solicited.

Having thus amended the claims to more specifically define the present invention, and having set forth in detail reasons why the invention as claimed is distinguishable over the prior art, Applicants submit that the application is now in condition for allowance and the early

issuance of a notice thereof is solicited. Should it appear that a telephone conference would expedite the allowance of the application, the Examiner is respectfully invited to contact the undersigned at the number set out below.

Date: June 12, 2002

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CERTIFICATE OF MAILING (37 CFR 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C., 20231.
Date: June 12, 2002

Vicki Naso

Version with markings to show changes made

In the Claims:

Please amend the claims as follows:

1. (Amended) A semiconductor device having at least one transistor, the device comprising:

a substrate having a channel region defined thereon;

a first insulating layer disposed over said channel region and over at least a portion of said substrate;

a floating gate generally disposed over said channel region and separated therefrom by said first insulating layer, said floating gate having at least two side walls and a top surface;

a second insulating layer disposed over said side walls and over said top surface of said floating gate;

a control gate having a first portion disposed over a portion of said [substrate] channel region and being separated therefrom by said second insulating layer, a second portion formed over a first one of said side walls and a third portion formed over at least a portion of said top surface of said floating gate and being separated from said floating gate by said second insulation layer, said second portion having a surface substantially parallel to and opposing said first side wall;

an erase gate formed over a second one of said side walls and over at least a portion of said top surface of said floating gate and being separated from said second one of said side walls by said second insulation layer;

a drain region formed in a portion of said substrate proximate said control gate; and

a source region formed in a portion of said substrate proximate said erase gate;

whereby during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored

electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process.

2. (Amended) A semiconductor device having at least one transistor as recited in claim 1 wherein said erase gate overlaps said floating gate and at least a portion of said control gate.

8. (Amended) A memory array disposed on a substrate comprising a plurality of memory cells each having a channel region formed in said substrate, a floating gate separated from said [substrate] channel region by a first insulating layer, an erase gate, a control gate separated from said floating gate by a second insulating layer, a source region, and a drain region, comprising:

a plurality of rows and columns of interconnected memory cells wherein the control gates of memory cells in the same row are connected by a common word-line, the erase gates of the memory cells in the same rows are connected by a common erase line, the source regions of the memory cells in the same rows are connected by a common source line, and the drain regions of memory cells in the same columns are commonly connected via a common drain line, wherein at least a portion of each said control gate is disposed over a portion of said [substrate] channel region and is separated therefrom by said second insulating layer, and wherein a portion of said control gate is [not] disposed [over] in facing relationship to a side surface of said floating gate and is separated therefrom by said second insulating layer; and

a control circuit connecting to said word-lines, erase lines, source lines and drain lines for operating one or more memory cells of said memory array;

whereby during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process.

9. (Amended) A memory array disposed on a substrate as recited in claim 8 wherein [each of said memory cells comprising: a substrate, a defined channel region, a] said floating

gate is generally disposed over said channel region and is separated therefrom by [a] said first insulating layer, [a] said control gate is generally placed on one side of said floating gate and separated therefrom by [a] said second insulation layer, [an] said erase gate is generally placed on a second side of said floating gate and is separated therefrom by said second insulation layer, [a] said drain region is generally disposed on [a first] said one side of said floating gate, and [a] said source region is generally disposed on [a] said second side of said floating gate.

10. (Amended) A memory array as recited in claim 9 wherein said erase gate overlaps said floating gate and at least a portion of said control gate.

16. (Amended) A semiconductor device having at least one transistor, the device comprising:

a substrate having a channel region;

a first insulating layer disposed over said channel region and over at least a portion of said substrate;

a floating gate generally disposed over said channel region and separated therefrom by said first insulating layer, said floating gate having at least two side walls and a top surface;

a second insulating layer disposed over said side walls and over said top surface of said floating gate;

a control gate having a first portion disposed over a portion of said [substrate] channel region and being separated therefrom by said second insulating layer, a second portion formed over a first one of said side walls and a third portion formed over at least a portion of said top surface of said floating gate and being separated from said floating gate by said second insulation layer, said second portion having a surface substantially parallel to and opposing said first one of said side walls;

an erase gate formed over a second one of said side walls and over at least a portion of said top surface of said floating gate and being separated from said second one of said side walls by said second insulation layer;

a source region formed in a portion of said substrate proximate said erase gate; and

a drain region formed in a portion of said substrate proximate said control gate;

whereby during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process.

17. (Amended) A semiconductor device having at least one transistor as recited in claim 16 wherein said erase gate is disposed over at least a portion of each of said floating gate and said control gate.

Add the following new claims:

18. (New) A semiconductor memory cell formed on a substrate, comprising:

a source region formed in said substrate;

first and second drain regions respectively formed in said substrate in spaced apart relationship to and on opposite sides of said source region;

a first channel region disposed between said first drain region and said source region, and a second channel region disposed between said source region and said second drain region;

a first floating gate having at least a substantial portion thereof disposed over said first channel region and separated therefrom by a first insulation layer, and a second floating gate having at least a substantial portion thereof disposed over said second channel region and separated therefrom by said first insulation layer;

an erase gate overlying said source region and having opposite extremities thereof extending over at least portions of said first and second floating gates; and

a first control gate having a first portion overlying said first channel region and a second portion overlying a portion of said first floating gate; and

a second control gate having a first portion overlying said second channel region and a second portion overlying a portion of said second floating gate;

whereby with said drain regions and erase gates grounded, a relatively high potential applied to said source region, and a relatively low potential applied to said control gates, the floating gates will be coupled to the high potential at the source region, and hot carriers produced in the channel regions under the floating gates and first portions of the control gates will be injected into the floating gates; and

whereby during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process.

19. (New) A memory cell as recited in claim 18 wherein each said floating gate has at least two side walls, and each said control gate has a third portion facing one of said side walls.

20. (New) A memory cell as recited in claim 19 wherein said erase gate has portions facing the other one of the sidewalls of each said floating gate.

21. (New) A memory cell as recited in claim 18 wherein each said floating gate has at least two side walls, and said erase gate has portions facing one of the side walls of each said floating gate.

22. (New) A memory cell as recited in claim 18 wherein said opposite extremities of said erase gate extend across said floating gates to overly portions of said first and second control gates.